# Assignment 1: Effect of parasitic capacitance

## Question 1: [10/100]

Write a basic description of the task. You can refer to the lecture notes for details of derivation (don’t reproduce it all!).

The task is divided into two main parts, the first part is the calculation of Fall time as a function of width and the second part is the calculation of fall time as a function of fan-out [1]. For each task, the load capacitance has to be recalculated, and the load capacitance is obtained by summing up several capacitances. It is therefore necessary to calculate all the capacitances required. However, when calculating the fall time for fan-out, the interconnect capacitance is ignored due to its relatively small value [2]. Both tasks use models built on 1.2 μm technology [1]. The calculation of the two fall times is presented in this question and the calculation for individual capacitance is presented in the fifth question.

**1.1 Fall time as a function of width (Unit fan-out)**

This task is to perform a transient analysis of the CMOS inverter, with a focus on the fall time for an inverter loaded with capacitor . The diagram for CMOS inverter can be seen below:

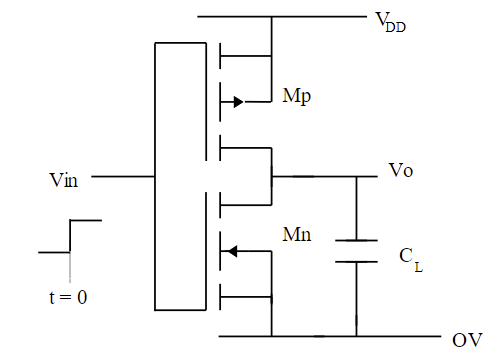


Figure 1: The CMOS inverter with an inverter load [3]

The here is the load capacitance of the following CMOS and the internal capacitances of the inverter. When t<0, the output of the inverter is logic high, which means is charged. When t=0, the input will change from logic low to logic high,which lead n-MOS turn on and discharge through n-MOS [1]. That makes the output voltage become low. For this task, the fall time needs to be calculated, which is the time between 90% VDD to 10% VDD as defined [3]. The figure for the fall time can be in the following figure.

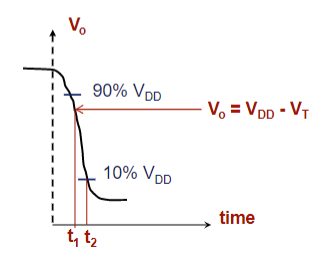


Figure 2: The fall time for the CMOS inverter [3]

As can be seen from the figure, the calculation of the fall time is divided into two parts, one for the time from 90% VDD to t1 and one for the time from t1 to 10% VDD (t2). The reason for this division is that the n-MOS is SATURATED during the 90%-t1 period because in this period. However, in the period t1-t2, as , the driver will be unsaturated, which means that different calculation formulas need to be used. Finally, the sum of the two times is the final Fall Time.

**1.1.1 The fall time for the driver is saturated**

When the driver is saturated, the current will be:

After rearraging the above equation and applying the integration with (-) limits, the fall time will be:

Thus,

When the driver is unsaturated, the current will be:

After rearranging the equation and applying the integration:

After soving the above equation, the fall time will be:

Therefore, the final fall time can be calculated by:

Substitute the above equations, the final fall time will be:

An important point that cannot be missed is the calculation of , which is made up of different capacitance. Therefore, the different capacitance values need to be accurately calculated and summed to obtain the final . The value for need be calculated by the combination of all capacitor shown below:

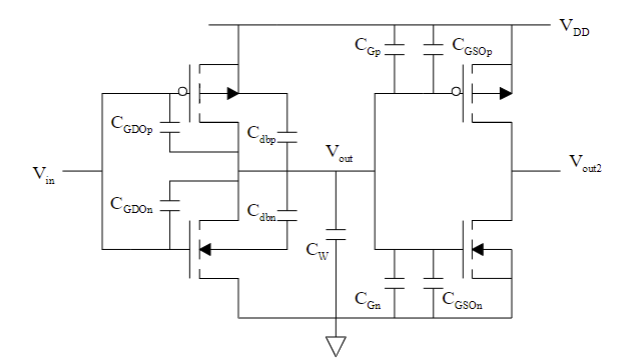


Figure 3: Unity fan-out CMOS converter [1]

Therefore, the capacitor will be:

Where, represents Gate-drain overlap capacitances, represents Gate-source overlap capacitances, represents Drain-body (substrate) capacitances, represents Total gate capacitances, represents Interconnect capacitance. The specific estimation and calculation of each capacitance will be placed in the next question.

In this task, the technology, **long-channel theory** and n-well process are all considered. For  a long-channel MOSFET, is negligibly small and it can be ignored. But for the short-channel MOSFET, the effect of can not be ignored. To simplify the calculations, this task uses long-channel theory, and the value of can be considered as a constant. Another reason for using long-channel theory can be seen in the next section. The lengths of the n-MOS and p-Mos will be both chosen as . And the width of p-MOS will be chosen to be 4 times the length of 1.2μm, which is 4.8 μm. For the variable width of the n-MOS, the range will be from and increased by 1.2μm each turn, i.e. , , , ….

**1.2 Fall time as a function of fan-out**

In this task, the number of inverters to the test inverter needs to be increased and the width will be fixed. With the increase of the number, the value of will also be increased. The diagram of Fan-out analysis can be seen below:

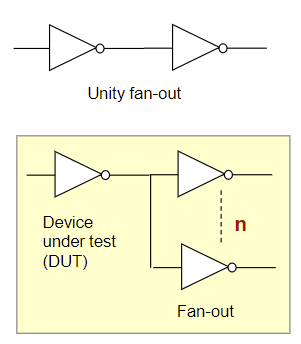
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Figure 4: The differences between the unity fan-out and fan out [3]

The effect of feeding more inverter gates can be investigated through the Fan-out analysis. Because the **long-channel theory** is applied in this task, the gate capacitance for instance will be more dominant than interconnect capacitance. Therefore, the effect of the interconnect capacitors can be ignored [3]. The following formula can be known:

Where, n is the number of inverters to the test, and W is the width of the MOSFET and L is the length of the MOSFET. The range of n will be chosen from 1 to 20.

## Question 2: [15/100]

Briefly describe the APPROXIMATIONS assumed in the analysis.

**2.1 Approximations for the fall time**

In this task, the fall time is defined as the time from 90%VDD to 10%VDD. But this range can be changed, in some other designs, the fall time will be from 70% to 30% [4]. Also, as can be seen from the figure above, the falling of the voltage starts earlier than 90% VDD. Therefore, the fall time in this task is only an estimation.

**2.2 Approximations for width and length for PMOS and NMOS**

Because the technology is used in this task, the length of NMOS and PMOS (L) will be the minimum feature size : . For unity fan-out ,the width of PMOS will be 4 (). Because the width of NMOS is variable, the range will be from 2 () to 20 ().

For fan-out, the width of NMOS will be a constant,which is 2() and the width of PMOS will be 4 (). The width of PMOS will be larger than that in NMOS. The reason is the difference of electron mobility is larger than hole mobility. To make the fall time and rise time is equal, the resistance of NMOS and PMOS should be the same. Therefore, the size of PMOS usually two or three times larger than NMOS size. When the length is equal, the width of PMOS will be two or three times larger than that in NMOS.

**2.3 Approximations for supply voltage and threshold voltage VT**

The value of will be assumed as 5V according to the lectures. Therefore , the will be =4.5V and will be =0.5V. The threshold voltage for NMOS will be 0.79V and for PMOS will be -0.91V [1]. Because long-channel theory is applied in this task, the will be not considered, which means the value of threshold will be a constant.

**2.4 Approximations for the current through of PMOS**

There is a small current in the p-channel device during fall time, but the current is relative small and can be ignored in this task [2]. Therefore, the current in the p-channel will be ignored.

**2.5 Approximations for capacitance for fan-out**

Because the value of interconnect capacitance is small compared with the gate capacitance, the interconnect capacitance will be ignored when calculating the load capacitance. Therefore, the value of load capacitance will be assumed as [3]. Due to the estimation of the load capacitor, the fall time for fan-out calculated from it is also influenced.

**2.6 Approximations for number of fan-out (n)**

Since it is not possible to place too many inverters at high speed, the number of inverters will be from 1 to 20 in this task. Alternatively, the number of inverters can be reduced to 1-10 for faster speed.

**2.7 Approximations for Drain-body (substrate) capacitance**

To calculate the value of Drain-body (substrate) capacitance, the value of and needs to be known, but the equation for the will be:

Because the value for is unknown, the above equation can not be used to calculate . The new factor needs to be considered. For the n-well doping, the value for NMOS and PMOS is different. We assume the n-well doping is 10 times higher than the substrate doping. Then, the non-linear capacitance above can be written as a linear capacitance , which can be expressed as . After calculating the value of and , the Drain-body (substrate) capacitance can be derived [1]. Similar to the reasons for , also makes a reasonable estimation.

**2.8 The use of unity fan-out when deriving the relationship between width and fall time**

To investigate the relationship between fall time and width of NMOS, the number of inverter will be one to control the variables.

**2.9 Approximations for interconnect capacitance**

As the Interconnect capacitance is very small, it was estimated to be 1fF when exploring the fall time and width of NMOS [1]. This capacitor was not considered when exploring the relationship between fall time and fan-out.

## Question 3 [20/100]

Include a graph of the Fall-time as a function of width, W. Use sensible range of values e.g. you can not drive many gates at high speed. Explain your graph/observations in the text box below the graph.

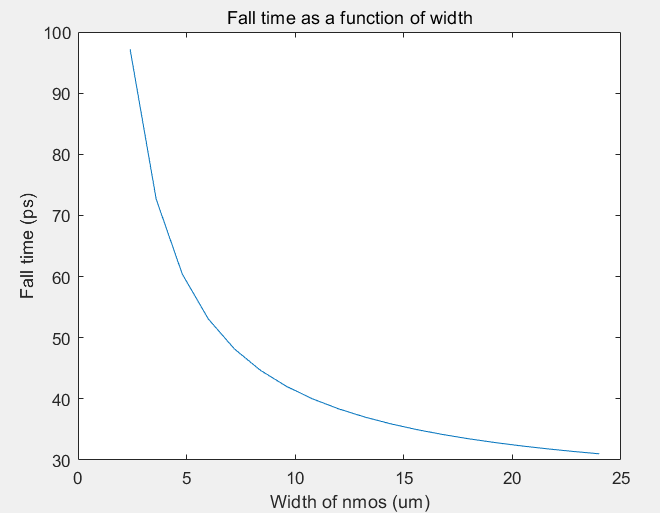


Figure 5: The Fall-time as a function of width

As can be seen from the graph above, the fall time as a function of width is an inverse proportional function. As the width of the NMOS increases, the fall time decreases, but at a slower rate. The width of NMOS ranges from to , where each increment is . In addition, for convenience, the width of NMOS is given in units of ，The unit for fall time is ps.

Since the fall time satisfies the following equation:

Therefore, the fall time will be linearly proportional to the load capacitance. As is calculated from the length and width of the MOS, the fall time will beinversely proportional to the drive constant, i.e. a large device (W/L) [2]. When the length is constant, the fall time will be inversely proportional to the width, as shown in the graph above. The reason is because

And and are proportional, so the fall time will be inversely proportional to .

Although the use of a larger device will increase the switching speed, it will also increase the capacitance.

## Question 4: [20/100]

Include a graph of Fall-time as a function of fan-out (i.e. attach an increasing number of inverters to the test inverter); choose one value of W. Explain your graph/observations in the text box below the graph.

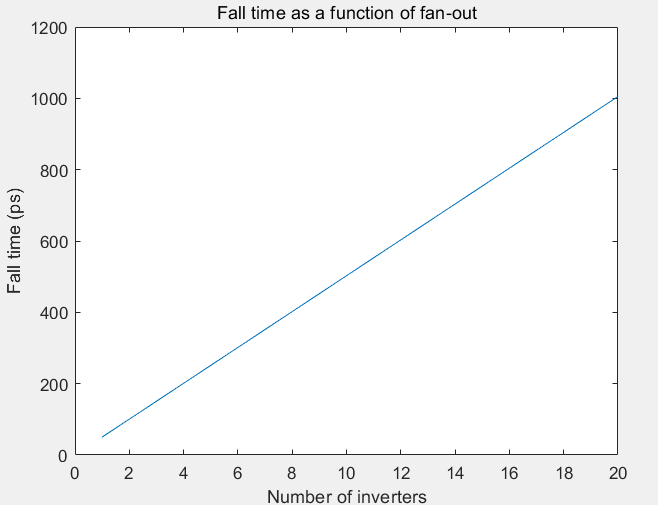


Figure : The Fall-time as a function of fan-out

From the above graph, the fall-time as a function of fan-out is a proportional function, which is as expected. Since a very large number of inverters at high speed cannot be used, the number of inverters set for this task is from 1 to 20. Similarly, the fall time is given in unit of ps for convenience of observation.

Since the interconnect capacitance is small compared to that of MOSFETs, only the total gate capacitance is taken into account when calculating the load capacitor. This results in a slightly lower fall time compared to the real value. The fall time when the number of inverters is 1 is less than 100ps, while the calculated fall time when considering the interconnect capacitance will be approximately 100ps (unity fan-out). However, the difference is acceptable. Similarly the fall time satisfies the following equation:

If substituting equations and =μ W/L to the above equation, the new equation will become [2]:

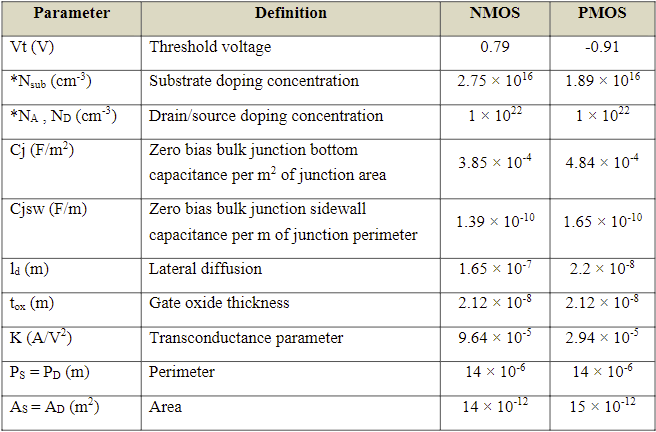
Because is constant, the fall time will be proportional to the number of inverters. It can also be seen from the above relationship that the importance of high mobility and shorter channel lengths for high speed applications.

## Question 5: [20/100]

List all your calculated device capacitance and other parameters. Which is the largest capacitance component? (remember how you should quote the values!)

The value of load capacitance can be calculated by the addition of different internal/external capacitances considering unity fan-out. The internal and external capacitance include: Gate-drain overlap capacitance, Gate-source overlap capacitance, Drain-body (substrate) capacitance, and total gate capacitance. The final comparison shows that the gate capacitance is the largest, especially the gate capacitance for PMOS. The specific parameter values can be seen in the following table.

Table 1: SPICE parameters for 1.2 μm CMOS technology [1]



Due to the need to use the international system of units, therefore, the substrate doping concentration for NMOS will be: , the substrate doping concentration for PMOS will be: . The Drain/Source doping concentration for NMOS will be: , The Drain/Source doping concentration for PMOS will also be: . The following section will calculate each type of capacitance using the values in the parameter table.

**5.1 Gate-drain overlap capacitance**

The gate (oxide) capacitance per unit area needs to be known first, the formula will be:

Then, the overlap capacitances CGDO and CGSO can be represented as:

For the NMOS, the overlap capacitance will be:

For the PMOS, the overlap capacitance will be:

Finally, the Gate-drain overlap capacitanve for NMOS and PMOS can be calculated by:

Because the value of is changed, only the equation will be provided.

**5.2 Gate-source overlap capacitance**

Similar to the calculation of Gate-drain overlap capacitance, the value of gate (oxide) capacitance per unit area also needs to be used.

For the NMOS, the overlap capacitance will be:

For the PMOS, the overlap capacitance will be:

Finally, the Gate-source overlap capacitance for NMOS and PMOS can be calculated by:

Because the value of is changed, only the equation will be provided.

**5.3 Drain-body (substrate) capacitance**

The built-in voltage needs to be calculated first, the equation will be:

Where is the intrinsic carrier concentration, which is .

For the NMOS, the value of will be , the built-in voltage will be:

For the PMOS, the doping will be a factor of 10 higher than the substrate doping because the n-well doping, therefore, the value of built-in voltage will be:

If the value of is assumed as 5V, then the high voltage will be 0.9\*VDD and the low voltage will be 0.1\*VDD, the factor will be:

Substituting the values yields, the factor for PMOS and NMOS will be:

Because the Drain-body capacitance can be calculated by:

Where is the zero bias bulk junction bottom capacitance per of junction area and is the Zero bias bulk junction sidewall capacitance per m of junction perimeter. The specific values for and can be seen in the table above.

Therefore, for the NMOS, the Drain-body capacitance will be:

For the PMOS, the Drain-body capacitance will be:

**5.4 Total gate capacitance**

The equation for calculating the total gate capacitance will be:

For the NMOS,

Because the value of is changed, only the equation will be provided.

For the PMOS,

**5.5 Load capacitance for unity fan-out**

Therefore, the final load capacitance can be calculated as:

If the width of NMOS is , the load capacitance wil be: .

**5.6 Load capacitance for fan-out**

The calculated the load capacitance is for unity fan-out, to find it when n>1, the following assumption is applied:

Because the long-channel theory is applied in this task, the gate capacitance for instance will be more important than interconnect capacitance. Therefore, the above equation can be satisfied. In this situation, the width of NMOS will be a constant and it is estimated as . The number of inverter gates will be from 1 to 20. Because a greater number of inverter gates is not practicable. Once the number of inverter gates is too large, the circuit will not work properly. The equation for the gate capacitance is same as before, which is:

Therefore, the final equation to calculate the load capacitance will be :

When n=1, the value of load capacitor will be: 1.41\*

**5.7 The largest capacitance component**

The comparison shows that total gate capacitance is the largest capacitance. For the total gate capacitance for PMOS, the gate capacitance is 9.38\* . This capacitance is much larger than the other capacitance, which is why only this capacitance is taken into account when calculating the load capacitance for fan-out.

**5.8 Calculate the Fall time**

After the value of the load capacitor has been calculated, the value of the capacitance needs to be applied to the formula for Fall time. As the equation for calculating Fall time is the same for unity fan-out and fan-out. The specific method for finding the Fall time can be seen in question 1, where the equation is as follows:

The threshold voltage of NMOS and PMOS are 0.79V and -0.91V, separately.

The value of can be calculated as:

Where is equal to the trans-conductance parameter, which is for NMOS and for PMOS. Therefore, for unity fan-out, only the width of NMOS is variable, all other parameters are constants. For fan-out, only the number of inverter is variable. Therefore, Fall time for each can be calculated and the graph can be simulated through MATLAB.

Question 6:[15/100]

Please paste your source code below. (If you right-click, paste options you choose to can keep the format as in, e.g. Matlab)

**6.1 Source code for fall time as a function of width**

%Threshold voltage for PMOS and NMOS (V)

Vtn=0.79;

Vtp=-0.91;

%Substrate doping concentration in SI units (m-3)

Nsubn=2.75e22;

Nsubp=1.89e22;

%Drain/source doping concentration in SI units (m-3)

NA=1e28;

ND=1e28;

%Zero bias bulk junction bottom capacitance per m2 of junction area (F/m2)

Cjn=3.85e-4;

Cjp=4.84e-4;

%Zero bias bulk junction sidewall capacitance per m of junction perimeter (F/m)

Cjswn=1.39e-10;

Cjswp=1.65e-10;

%Lateral diffusion for NMOS and PMOS (m)

ldn=1.65e-7;

ldp=2.2e-8;

%Gate oxide thickness for NMOS and PMOS (m)

toxn=2.12e-8;

toxp=2.12e-8;

%Transconductance parameter for NMOS and PMOS (A/V2)

Kn=9.64e-5;

Kp=2.94e-5;

%Perimeter for NMOS and PMOS (m)

Psn=14e-6;

Pdn=14e-6;

Psp=14e-6;

Pdp=14e-6;

%Area for NMOS and PMOS (m2)

Asn=14e-12;

Adn=14e-12;

Asp=15e-12;

Adp=15e-12;

%Intrinsic carrier concentration (m-3)

ni=1.5e16;

%Permittivity of free space (F/m)

per0=8.85e-12;

%Relative permittivity

perox=3.9;

%Supply voltage (V)

VDD=5;

%Interconnect capacitance in SI unit (F)

Cw=1e-15;

%The length of NMOS and PMOS (m)

Ln=1.2e-6;

Lp=1.2e-6;

%The width of NMOS and PMOS (m). The range of Wn will be from

%2.4um to 24um

Wp=4.8e-6;

Wn=(2.4e-6:1.2e-6:24e-6);

%High voltage and low voltage for calculating the factor Keq

VH=0.9\*VDD;

VL=0.1\*VDD;

%Gate oxide capacitance per unit area (F/m2)

C\_on=((per0\*perox)/toxn);

C\_op=((per0\*perox)/toxp);

%Total gate capacitance for NMOS and PMOS (F)

C\_Gn=C\_on\*Wn\*Ln;

C\_Gp=C\_op\*Wp\*Lp;

%Built-in voltage for NMOS and PMOS (V)

Vbin=0.025\*log((NA\*Nsubn)/(ni^2));

Vbip=0.025\*log((NA\*Nsubp\*10)/(ni^2));

%The factor Keq for NMOS and PMOS to calculating the Drain-body (substrate) capacitance

Keqn=((Vbin^0.5)/((VH-VL)\*0.5))\*((abs(Vbin+VH))^0.5-(abs(Vbin+VL))^0.5);

Keqp=((Vbip^0.5)/((VH-VL)\*0.5))\*(((abs(Vbip+VH)))^0.5-(abs(Vbip+VL))^0.5);

%Drain-body (substrate) capacitance for NMOS and PMOS (F)

Cdbn=Keqn\*(Adn\*Cjn+Pdn\*Cjswn);

Cdbp=Keqp\*(Adp\*Cjp+Pdp\*Cjswp);

%Overlap capacitances: CGDO, CGSO (F/m) for NMOS and PMOS (F/m)

CGDOn=C\_on\*ldn;

CGSOn=C\_on\*ldn;

CGDOp=C\_op\*ldp;

CGSOp=C\_op\*ldp;

%Gate-drain overlap capacitance for NMOS and PMOS (F)

C\_GDOn=2\*CGDOn\*Wn;

C\_GDOp=2\*CGDOp\*Wp;

%Gate-source overlap capacitance for NMOS and PMOS (F)

C\_GSOn=CGSOn\*Wn;

C\_GSOp=CGSOp\*Wp;

%Load capacitance (F)

CL=C\_GSOn+C\_GSOp+C\_GDOn+C\_GDOp+Cdbn+Cdbp+C\_Gn+C\_Gp+Cw;

%The value of beta

betan=Kn\*Wn/Ln;

%Fall time as a function of width for unity fan-out

Fall\_time=CL./(betan\*(VDD-Vtn))\*(2\*(Vtn-0.1\*VDD)/(VDD-Vtn)+log((2\*(VDD-Vtn)-0.1\*VDD)/(0.1\*VDD)));

%Plot the relationship for the fall time as a function of width

plot(Wn\*1e6,Fall\_time\*1e12);

xlabel('Width of nmos (um)'); %label X axis

ylabel('Fall time (ps)'); %label Y axis

title('Fall time as a function of width'); %provide title

6.2 **Source code for fall time as a function of fan-out**

%Threshold voltage for PMOS and NMOS (V)

Vtn=0.79;

Vtp=-0.91;

%Substrate doping concentration in SI units (m-3)

Nsubn=2.75e22;

Nsubp=1.89e22;

%Drain/source doping concentration in SI units (m-3)

NA=1e28;

ND=1e28;

%Zero bias bulk junction bottom capacitance per m2 of junction area (F/m2)

Cjn=3.85e-4;

Cjp=4.84e-4;

%Zero bias bulk junction sidewall capacitance per m of junction perimeter (F/m)

Cjswn=1.39e-10;

Cjswp=1.65e-10;

%Lateral diffusion for NMOS and PMOS (m)

ldn=1.65e-7;

ldp=2.2e-8;

%Gate oxide thickness for NMOS and PMOS (m)

toxn=2.12e-8;

toxp=2.12e-8;

%Transconductance parameter for NMOS and PMOS (A/V2)

Kn=9.64e-5;

Kp=2.94e-5;

%Perimeter for NMOS and PMOS (m)

Psn=14e-6;

Pdn=14e-6;

Psp=14e-6;

Pdp=14e-6;

%Area for NMOS and PMOS (m2)

Asn=14e-12;

Adn=14e-12;

Asp=15e-12;

Adp=15e-12;

%Intrinsic carrier concentration (m-3)

ni=1.5e16;

%Permittivity of free space (F/m)

per0=8.85e-12;

%Relative permittivity

perox=3.9;

%Supply voltage (V)

VDD=5;

%Interconnect capacitance in SI unit (F)

Cw=1e-15;

%The length of NMOS and PMOS (m)

Ln=1.2e-6;

Lp=1.2e-6;

%The width of NMOS and PMOS (m)

Wp=4.8e-6;

Wn=2.4e-6;

%High voltage and low voltage for calculating the factor Keq (V)

VH=0.9\*VDD;

VL=0.1\*VDD;

%The number of inveters. The range will be from 1 to 20.

n=1:1:20;

%Gate oxide capacitance per unit area (F/m2)

C\_on=((per0\*perox)/toxn);

C\_op=((per0\*perox)/toxp);

%Total gate capacitance for NMOS and PMOS (F)

C\_Gn=C\_on\*Wn\*Ln;

C\_Gp=C\_op\*Wp\*Lp;

%Built-in voltage for NMOS and PMOS (V)

Vbin=0.025\*log((NA\*Nsubn)/(ni^2));

Vbip=0.025\*log((NA\*Nsubp\*10)/(ni^2));

%The factor Keq for NMOS and PMOS to calculating the Drain-body (substrate) capacitance

Keqn=((Vbin^0.5)/((VH-VL)\*0.5))\*((abs(Vbin+VH))^0.5-(abs(Vbin+VL))^0.5);

Keqp=((Vbip^0.5)/((VH-VL)\*0.5))\*(((abs(Vbip+VH)))^0.5-(abs(Vbip+VL))^0.5);

%Drain-body (substrate) capacitance for NMOS and PMOS (F)

Cdbn=Keqn\*(Adn\*Cjn+Pdn\*Cjswn);

Cdbp=Keqp\*(Adp\*Cjp+Pdp\*Cjswp);

%Overlap capacitances: CGDO, CGSO (F/m) for NMOS and PMOS (F/m)

CGDOn=C\_on\*ldn;

CGSOn=C\_on\*ldn;

CGDOp=C\_op\*ldp;

CGSOp=C\_op\*ldp;

%Gate-drain overlap capacitance for NMOS and PMOS (F)

C\_GDOn=2\*CGDOn\*Wn;

C\_GDOp=2\*CGDOp\*Wp;

%Gate-source overlap capacitance for NMOS and PMOS (F)

C\_GSOn=CGSOn\*Wn;

C\_GSOp=CGSOp\*Wp;

%Load capacitance (F)

CL=n.\*(C\_Gp+C\_Gn);

%The value of beta

betan=Kn\*Wn/Ln;

%Fall time as a function of width for fan-out

Fall\_time=CL./(betan\*(VDD-Vtn))\*(2\*(Vtn-0.1\*VDD)/(VDD-Vtn)+log((2\*(VDD-Vtn)-0.1\*VDD)/(0.1\*VDD)));

%Plot the relationship for the fall time as a function of fan-out

plot(n,Fall\_time\*1e12);

xlabel('Number of inverters'); % to label X axis

ylabel('Fall time (ps)'); % to label Y axis

title('Fall time as a function of fan-out'); %to provide title to your plot

**References**

[1] K. Hoettges, “Integrated Circuit Design Assignment 1”, [Online]. Available: <https://liverpool.instructure.com/courses/58614>

[2] M.Raja, “Lecture 7 (Part I): Transient analysis of CMOS”, [Online]. Available: <https://liverpool.instructure.com/courses/58614>

[3] M.Raja, “Assignment 1 –Hints/Tips”, [Online]. Available: <https://liverpool.instructure.com/courses/58614>

[4] VLSI System Design, “Propagation Delay of CMOS inverter”, [Online]. Available: https://www.vlsisystemdesign.com/propagation-delay-of-cmos-inverter/